

What is claimed is

1. A supporting structure for a chip, comprising:
 - 5 a supporting substrate with a bond opening therein; an interconnect layer on the supporting substrate, in which a bonding channel overlapping with the bond opening is formed; and
 - 10 an escape prevention structure for the bonding channel, to enable escaping of air from the bonding channel and to prevent the encapsulation material from escaping from the bonding channel on introducing encapsulation material into the bonding channel after the applying of a chip to the supporting structure.
2. The supporting structure of claim 1, wherein the escape prevention structure is designed to prevent escaping of the encapsulation material due to the capillary effect.
- 20 3. The supporting structure of claim 1, wherein the escape prevention structure includes an opening with such a cross-sectional area, so that escaping of the encapsulation material caused by the capillary effect is prevented.
- 25 4. The supporting structure of claim 1, wherein the bonding channel is open at a lateral end, wherein the escape prevention structure is formed at the lateral end by a barrier structure for reducing a cross-section of the bonding channel at the lateral end.
- 30 5. The supporting structure of claim 4, wherein the barrier structure is connected to the interconnect layer.

6. The supporting structure of claim 4, wherein the barrier structure is formed integrally with the interconnect layer.
- 5 7. The supporting structure of claim 4, wherein the barrier structure extends across the entire width of the bonding channel.
- 10 8. The supporting structure of claim 4, wherein the barrier structure is formed, so that a cross-section of the bonding channel tapers in a direction to the lateral end.
9. The supporting structure of claim 4, wherein the barrier structure has a convex shape.
- 15 10. The supporting structure of claim 4, wherein the barrier structure is disposed in the bonding channel and spaced from the interconnect layer.
- 20 11. The supporting structure of claim 1, wherein the escape prevention structure includes a recess in the supporting substrate.
- 25 12. The supporting structure of claim 11, wherein the bonding channel is laterally completely closed.
- 30 13. The supporting structure of claim 11, wherein the interconnect layer is disposed on a surface of the supporting substrate, wherein the recess on the surface extends across a sidewall of the bonding channel.
- 35 14. The supporting structure of claim 11, wherein the recess is disposed in a region of the bonding channel, wherein the recess extends from a first surface of the supporting substrate to a second surface of the supporting substrate.

15. The supporting structure of claim 1, wherein a chip is disposed on the interconnect layer.

16. A method for producing a supporting structure for a
5 chip, comprising:

preparing a supporting substrate with a bond opening;

10 creating an interconnect layer on the supporting substrate, so that a bonding channel is formed in the interconnect layer; and

15 creating an escape prevention structure for the bonding channel, so that the escape prevention structure is formed to enable escaping of air from the bonding channel and to prevent the encapsulation material from escaping from the bonding channel on introducing encapsulation material into the bonding channel after the applying of a chip to the
20 interconnect layer.

17. The method of claim 16, wherein the step of creating an interconnect layer includes creating a frame on the supporting substrate, and the step of creating an escape prevention structure includes deepening the frame for forming a vent flute in the frame

18. The method of claim 16, wherein the step of creating an interconnect layer comprises creating a frame on the supporting substrate, and the step of creating an escape prevention structure comprises the step of applying a spacer to the frame.

19. The method of claim 16, wherein the step of creating an interconnect layer includes structuring the interconnect layer and subsequently depositing the structured interconnect layer onto the supporting substrate.

20. The method of claim 16, wherein the step of creating an interconnect layer includes printing the interconnect layer onto the supporting substrate.

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21. The method of claim 16, wherein the step of creating the interconnect layer includes creating an interconnect layer with a bonding channel with a lateral open end, and the step of creating the escape prevention structure 10 includes creating a barrier structure at the lateral open end.

22. The method of claim 21, wherein the step of creating the interconnect layer and the step of creating a barrier 15 structure take place concurrently.